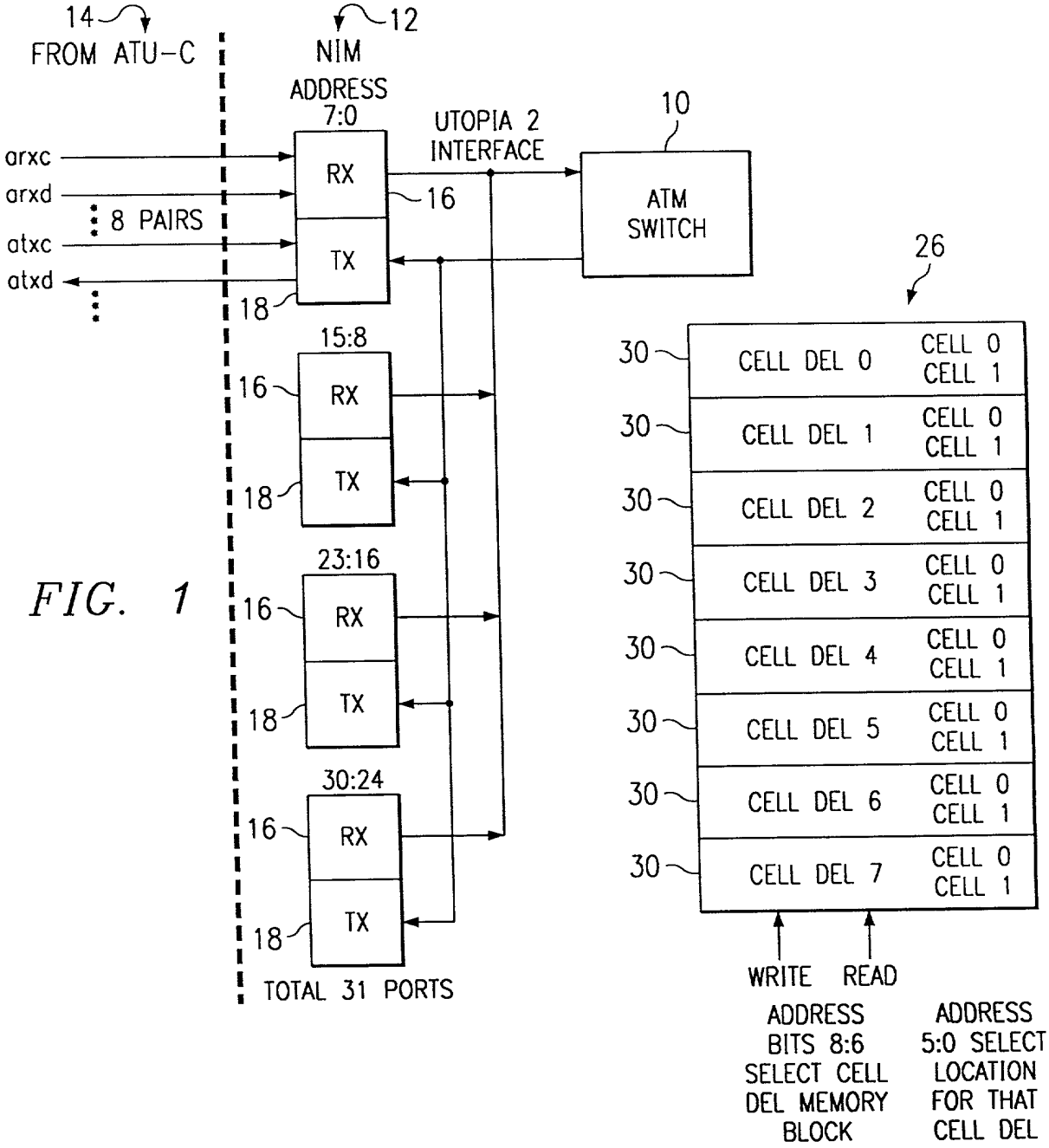


FIG. 1

FIG. 3

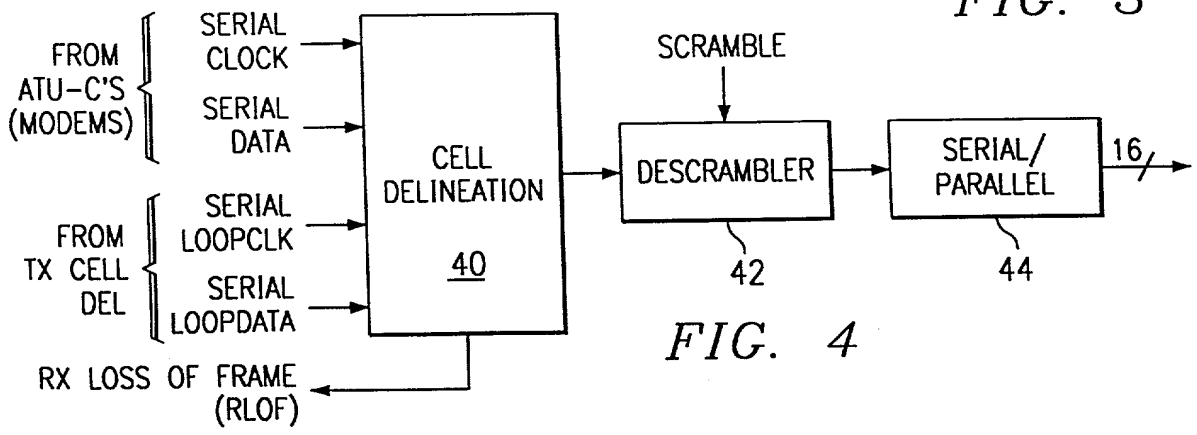


FIG. 4

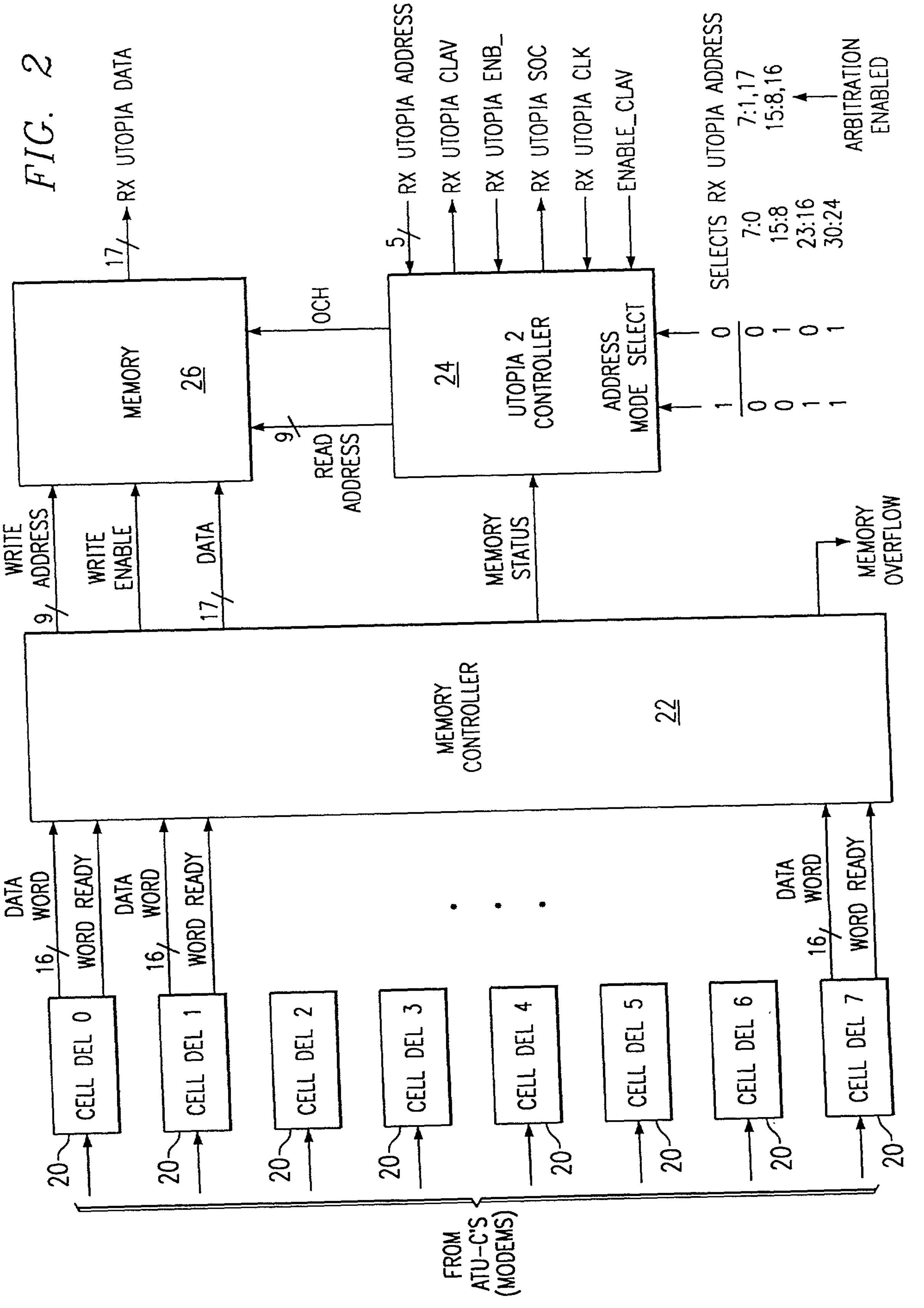
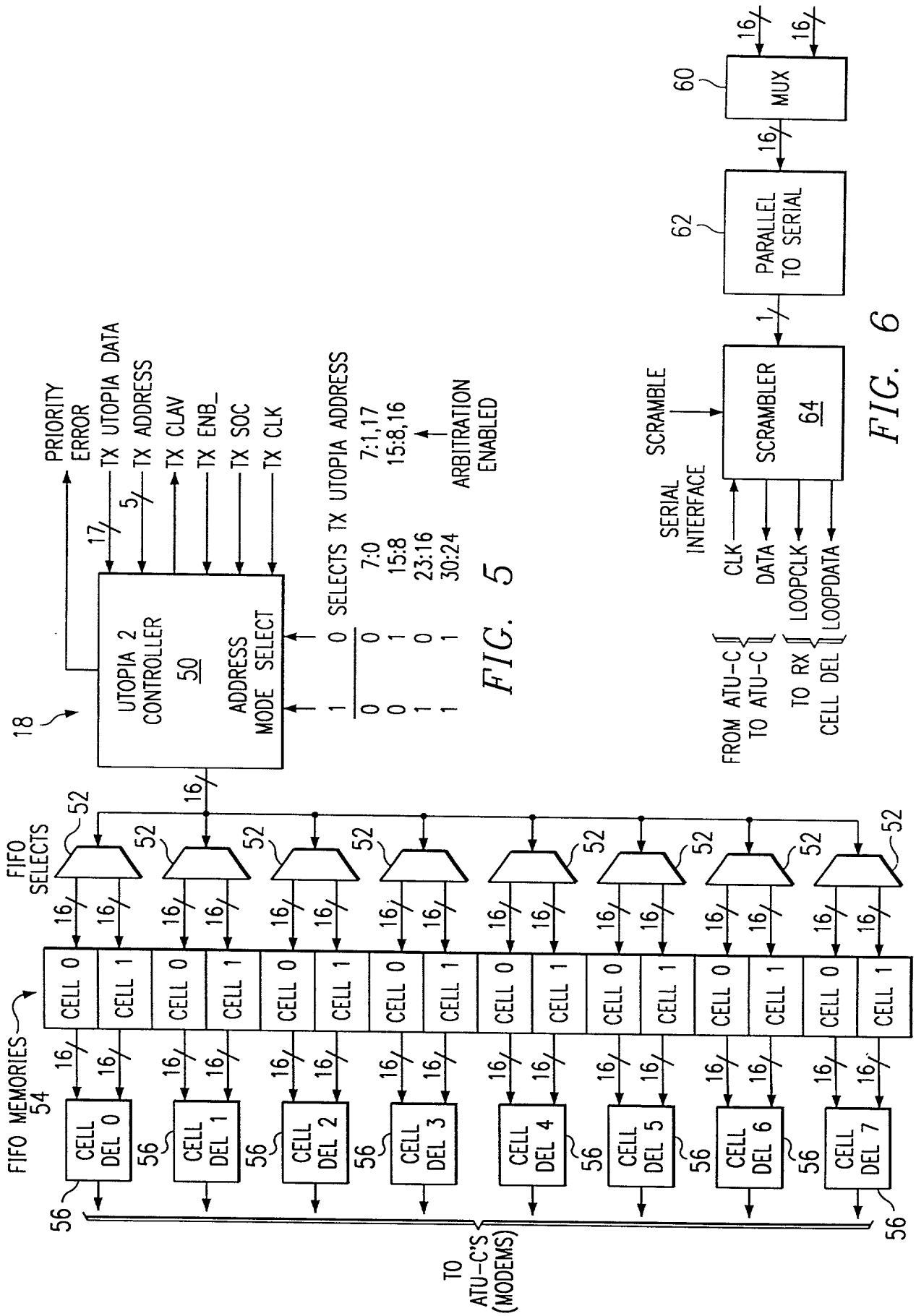

MEMORY
26
RX UTOPIA DATA
17
WRITE ADDRESS
WRITE ENABLE
DATA
9
17
OCH
READ ADDRESS
9
UTOPIA 2 CONTROLLER
24
ADDRESS MODE SELECT
RX UTOPIA ADDRESS
5
RX UTOPIA CLAV
RX UTOPIA ENB_
RX UTOPIA SOC
RX UTOPIA CLK
ENABLE_CLAV
1 0 SELECTS RX UTOPIA ADDRESS
0 0 7:0
0 1 15:8 7:1,17
1 0 23:16 15:8,16
1 1 30:24
ARBITRATION ENABLED
MEMORY STATUS
MEMORY OVERFLOW
MEMORY CONTROLLER
22
DATA WORD
16
WORD READY
CELL DEL 0
CELL DEL 1
CELL DEL 2
CELL DEL 3
CELL DEL 4
CELL DEL 5
CELL DEL 6
CELL DEL 7
20
FROM ATU-C'S (MODEMS)

FIG. 2


PRIORITY ERROR
TX UTOPIA DATA
TX ADDRESS
TX CLAV
TX ENB_
TX SOC
TX CLK
17
5
18
UTOPIA 2 CONTROLLER 50
ADDRESS MODE SELECT
1 0 SELECTS TX UTOPIA ADDRESS
0 0 7:0 7:1,17
0 1 15:8 15:8,16
1 0 23:16
1 1 30:24
ARBITRATION ENABLED
FIG. 5
SCRAMBLE
SERIAL INTERFACE
SCRAMBLER 64
CLK
DATA
LOOPCLK
LOOPDATA
FROM ATU-C
TO ATU-C
TO RX
CELL DEL
PARALLEL TO SERIAL
MUX
60
62
16
1
FIFO SELECTS
52
FIFO MEMORIES 54
CELL 0
CELL 1
CELL DEL 0
CELL DEL 1
CELL DEL 2
CELL DEL 3
CELL DEL 4
CELL DEL 5
CELL DEL 6
CELL DEL 7
56
TO ATU-C'S (MODEMS)
FIG. 6